Effects of Arsenic Concentration Profile on Electric Properties of Gate Oxide in MOS Devices

K.-S. Chang-Liao and C.-S. Chuang
Department of Engineering and System Science,
National Tsing Hua University,
Hsinchu 30013, TAIWAN, ROC

The effects of arsenic concentration profiles in gate oxide on the electrical properties of metal-oxide-Si (MOS) capacitors were investigated. It is found that arsenic in the gate oxide bulk degrades the electric property of MOS devices. Interestingly, the electric property of MOS devices can be improved by an increase of arsenic concentration at the SiO_2/Si interface. This improvement may be attributed to the interfacial strain relaxation and/or the replacement of non-bridging bonds. The arsenic concentration profile in gate oxide plays a crucial role on the electric property of MOS devices.

Impurity in the gate oxide is a key issue for a metal-oxide-silicon (MOS) device as the gate oxide thickness is gradually decreased. The n^+ poly-Si gate doped by As^+ implantation has been shown to be suitable for practical use in MOS devices. It was reported that the As^+ poly-Si gate is very stable because of little flat-band voltage shift (ΔV_{fb}) in the MOS capacitor after long-term bias temperature aging tests [1]. Other researchers have found that the MOS device with an As-doped gate can achieve a high charge-to-breakdown (Q_{bd}) and a small poly-Si depletion by doping high concentrations of As [2]. These advantages are due to the little segregation of As in the gate oxide. However, it has been observed that the long-term avalanche injection induced ΔV_{fb} in the MOS device with an As-doped gate is significantly increased [1]. And the reliability degradation of MOS device was caused by a arsenic diffusion into gate oxide[3]. Thus, the claim that the stability and reliability of MOS devices with the As-doped gate are superior is disputable. Since the As-doped poly-Si gate is generally used for n-channel MOS transistors, the electrical properties of the MOS capacitor with As-doped gate deserve to be studied further.

After arsenic ions (As^+) implantation, the samples were annealed in N_2 at 900 ℃ for 10, 20, 30 min (i.e., sample 910, 920, 930, respectively), and at 1000 ℃ for 10, 20, 30 min (i.e., sample 1010, 1020, 1030, respectively). The SIMS profiles of arsenic concentration in gate oxides with various post-implantation annealing conditions for oxide thicknesses of 50 and 35Å are shown in Figure 1(a) and 1(b), respectively. For gate oxide thickness of 50Å, arsenic concentration in oxide bulk is mainly increased with the increase in annealing temperature/time. This can be well understood by the drive-in diffusion of arsenic from gate electrode. As for gate oxide thickness of 35Å, arsenic concentration is larger and the profiles are closer to the SiO_2/Si interface as compared with those of 50Å. It is noted that the arsenic concentration at the SiO_2/Si interface is increased with the increase in annealing temperature/time. Therefore from Fig. 1(a) and 1(b), the arsenic profiles in gate oxide are strongly dependent on the gate oxide thickness and the post-implantation annealing conditions.

Figure 2 shows the leakage current of gate oxides with various post-implantation annealing for oxide thicknesses of (a) 50 and (b) 35Å, respectively. For gate oxide thickness of 50Å, leakage current is increased with the increase in annealing temperature/time. This could be due to a larger amount of arsenic in gate oxide for a higher temperature and/or longer time of post-implantation annealing. As for gate oxide thickness of 35Å, by contrast, leakage current is decreased with the increase in post-implantation annealing temperature/time. This leakage current behavior may be correlated to arsenic concentration at the SiO_2/Si interface. The leakage current in gate oxide can be decreased with the increase of arsenic concentration at the SiO_2/Si interface although an increase of arsenic concentration in the oxide bulk may cause some detrimental effects on electric property as described above. It has been reported that a pileup of nitrogen at SiO_2/Si interface is beneficial to the electric property improvement in MOS device [4]. This was explained by the interfacial strain relaxation and the replacement of non-bridging bonds and/or defects. Therefore, by a similar physical mechanism, the electric property improvement due to an increase of arsenic concentration at SiO_2/Si interface can be reasonably explained.

[1] M. Itsumi et al., *J. Appl. Phys.*, **73**(11), 1993, p.7515.
[2] A. I. Chou et al., *Appl. Phys. Lett.*, **69**, 1996, p.934.
[3] K.S. Chang-Liao and C.-H. Chen, *Jpn. J. Appl. Phys.*, **37**, 1998, p. L1224.
[4] K.S. Chang-Liao and H.-C. Lai, *Appl. Phys. Lett.*, **72**(18)**,** 1998, p.2280.

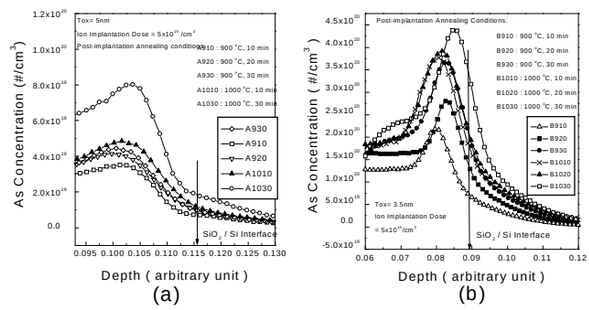

Fig. 1 SIMS profiles of arsenic concentration in gate oxides with various post-implantation annealing conditions for oxide thicknesses of (a) 50Å and (b) 35Å.

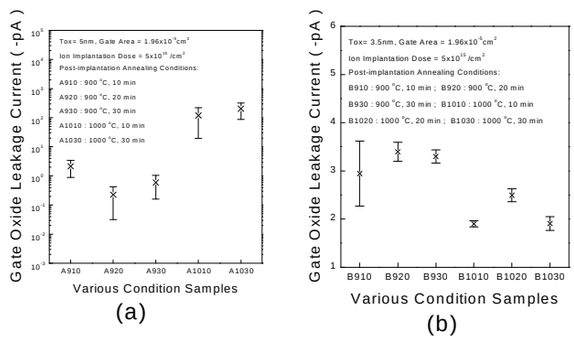

Fig. 2 Leakage current of gate oxides with various post-implantation annealing for oxide thicknesses of (a) 50Å and (b) 35Å.